SOLAPURUNIVERSITY,SOLAPUR

FACULTY OF ENGINEERING & TECHNOLOGY

ELECTRONICS ENGINEERING

CBCS Syllabus for

First Year M.Tech.
w.e.f. Academic Year 2018-19

SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY

STRUCTURE OF M.Tech. (ELECTRONICS ENGINEERING)

Four Semester Course

Choice Based Credit System Syllabus wef 2018 -19

Semester-I

Sr. No.	*Subject*	*Teaching Scheme*				*Credits*				*Evaluation Scheme*				
		L	*T*	*P*	*Total*	*Credits (L)*	*Credits (T)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA- P Marks*	*ICA-T Marks*	*Total Marks*
1	Digital Design and Verification	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
2	Advanced Digital Signal Processing	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
3	Voice and Data Networks	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
4	Machine Learning©	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
5	Elective I	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
6	Seminar- I	-	-	2	2	-	-	2.0	2.0	ISE	--	50	--	50
										ESE	--	--	--	
Total		**15**	**2**	**8**	**25**	**15.0**	**2.0**	**5.0**	**22.0**		**500**	**125**	**50**	**675**

Note : *L- Lectures, P-Practical, T-Tutorial, ISE- In Semester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment*

© - This Course is common for M.Tech. (Electronics Engineering) and M.Tech. (Computer Science & Engineering)

SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY

STRUCTURE OF M.Tech. (ELECTRONICS ENGINEERING)

Four Semester Course

Choice Based Credit System Syllabus wef 2018-19

Semester-II

Sr. No.	*Subject*	*Teaching Scheme*				*Credits*				*Evaluation Scheme*				
		L	*T*	*P*	*Total*	*Credits (L)*	*Credits (T)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA- P Marks*	*ICA-T Marks*	*Total Marks*
1	Research Methodology & IPR©	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
2	Communication Buses & Interfaces	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
3	Advanced IOT	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
4	PLC, SCADA and Distributed Control Systems	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
5	Elective – II	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
6	Seminar- II	-	-	2	2	-	-	2.0	2.0	ISE	--	50	--	50
										ESE	--	--	--	
Total		**15**	**2**	**8**	**25**	**15.0**	**2.0**	**5.0**	**22.0**		**500**	**125**	**50**	**675**

Note : *L- Lectures, P-Practical, T-Tutorial, ISE- In Semester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment*

© - This Course is common for M.Tech. (Electronics Engineering) and. M.Tech. (Computer Science & Engineering)

- Seminar I shall be delivered on a topic related to student's broad area of interest for dissertation work selected in consultation with the advisor after compiling the information from the latest literature. Student shall deliver seminar using modern presentation tools. A hard copy of the report (as per format specified by the department) shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.

- Seminar II shall be delivered on a topic related to student's particular area of interest for dissertation work selected in consultation with the advisor after compiling the information from the latest literature. Student shall deliver seminar using modern presentation tools. A hard copy of the report (as per format specified by the department) shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.

- **List of elective courses for semester I and II -**

Sr.	*Elective - I*	*Elective – II*
1	Wireless Sensor Networks	Mobile Technology
2	Analog & Digital CMOS VLSI Design	Real Time Systems
3	Image and Video Processing	VLSI in Signal Processing
4	Neural Networks & Fuzzy Control Systems	Advanced Control Systems

- Courses may be added in the list of Elective I and II as and when required

SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY
STRUCTURE OF M.E. (ELECTRONICS ENGINEERING)
Four Semester Course
Choice Based Credit System Syllabus
Semester-III

Sr. No.	*Subject*	*Teaching Scheme*		*Credits*			*Evaluation Scheme*			
		L	*P*	*Credits (L)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA Marks*	*Total Marks*
1	Self Learning Course	$	-	3.0	-	3.0	ISE	30	--	100
							ESE	70		
2	Open Elective Course#	3		3.0		3.0	ISE	30		100
							ESE	70		
3	Dissertation Phase I : Synopsis Submission Seminar*		@4		3.0	3.0	ISE	--	100	100
							ESE	--	--	
4	Dissertation Phase II : ICA*		-		3.0	3.0	ISE	--	100	100
							ESE	--	--	
5	Dissertation Phase II Progress Seminar*		-		3.0	3.0	ISE	--		100
							ESE	--	100	
Total		**3**	**4**	**6.0**	**9.0**	**15.0**		**200**	**300**	**500**

L- Lectures, P-Practical, T-Tutorial, ISE- In Semester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment

Note -

- $- Being a Self Learning Course, student shall prepare for examination as per specified syllabus
- *- For all activities related to dissertation Phase I (synopsis submission seminar and progress seminar) student must interact regularly every week with the advisor.
- # - This course is common for all branches of Technology (ie for all M.Tech. Programs)

- Synopsis submission seminar shall cover detailed synopsis of the proposed work. Student shall submit synopsis of the dissertation work only after delivering this seminar.
- Progress seminar shall be delivered capturing details of the work done by student for dissertation
- Student shall deliver all seminars using modern presentation tools. A hard copy of the report shall be submitted to the department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any
- @ Indicates contact hours of students for interaction with advisor.
- Details of modes of assessment of seminar and dissertation shall be as specified in 7(III) of PG Engineering Ordinance of Solapur University, Solapur

List Self Learning Courses -

Sr.	***Self LearningSubject***
1	Network and Internet Security
2	Programmable System on Chip (PSoC)
3	Soft Computing
4	Advanced Process Control

List of Open Elective Courses-

Sr.	***Self LearningSubject***
1	Business Analytics
2	Operation Research
3	Cost Management of Engineering Projects
4	Non Conventional Energy

- New Self Learning Courses and New Open Elective Courses may be added as and when required

SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY
STRUCTURE OF M.E. (ELECTRONICS ENGINEERING)
Four Semester Course
Choice Based Credit System Syllabus
Semester-IV

Sr. No.	*Subject*	*Teaching Scheme*			*Credits*			*Evaluation Scheme*		
		L	*P*	*Total*	*Credits (L)*	*Credits (P)*	*Total Credits*	*Scheme*	*ICA Marks*	*Total Marks*
1	Dissertation Phase III : Progress Seminar #	-	4@	4	-	3.0	3.0	ISE	100	100
2	Dissertation Phase IV: #	-	2@	2	-	6.0	6.0	--	200	200
3	Final Submission of the Dissertation and Viva –Voce	-	-	-	-	6.0	6.0	ESE	200	200
	Total	**-**	**-**	**6**	**--**	**15.0**	**15.0**	**-**	**500**	**500**

Note –

- #- For all activities related to dissertation Phase III & IV student must interact regularly every week with the advisor.
- Progress seminar shall be delivered capturing details of the work done by student for dissertation
- Student shall deliver all seminars using modern presentation tools. A hard copy of the report shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.
- Student must submit a hard copy of Project Report to the department
- @ indicates contact hours of the student for interaction with the advisor
- Details of modes of assessment of seminar and dissertation shall be as specified in 7 (III) of PG Engineering Ordinance of Solapur University, Solapur.

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

DIGITAL DESIGN AND VERIFICATION

Teaching Scheme	Examination Scheme
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Revision of Basic Digital Systems **(6 Hrs)**

Combinational circuits, sequential circuits, logic families, synchronous FSM and asynchronous design, metastability, clock distribution and issues, basicbuilding blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, barrel shifter etc.

Unit 2: Verilog / VHDL **(7 Hrs)**

Verilog/VHDL comparisons and guidelines, Verilog: HDL fundamentals, simulation, and testbench design, examples of Verilog codes for combinational and sequential logic, Verilog AMS

Unit 3:System Verilog and Verification: **(8 Hrs)**

Verification guidelines, data types, procedural statements and routines, connecting the test bench and design, assertions, basic OOP concepts, randomization, introduction to basic scripting language: Perl, Tcl/Tk

SECTION II

Unit 4: Current Challenges in Physical Design: **(8 Hrs)**

Roots of challenges, delays: wire load models generic PD flow, challenges in PD flow at different steps, SI challenge - noise & crosstalk, IR drop, Process effects: process antenna effect & electro migration

Unit 5: Programmable Logic Devices: **(6 Hrs)**

Introduction, evolution: PROM, PLA, PAL, architecture of PAL's, applications, programming PLD's, FPGA with technology: antifuse, SRAM, EPROM, MUX, FPGA structures, and ASIC design flows, programmable interconnections, coarse grainedreconfigurable devices

Unit 6: IP and Prototyping: **(7 Hrs)**

IP in various forms: RTL source code, encrypted source code, soft IP, netlist, physical IP, and use of external hard IP during prototyping, case studies and speedissues, testing of logic circuits: fault models, BIST, JTAG interface

- **Internal Continuous Assessment (ICA)**
  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum

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- **Reference Books**

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone publications, 1998.
2. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall,
3. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press
4. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer
5. Janick Bergeron, “Writing Testbenches: Functional Verification of HDL Models”, Second Edition, Springer

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

ADVANCED DIGITAL SIGNAL PROCESSING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA **–** 25Marks

SECTION-I

Unit 1: Design of Digital Filters (07 Hrs)

Overview of DSP, characterization in time and frequency, FFT Algorithms, digital filter design and structures: basic FIR/IIR filter design & Structures, design techniques of linear phase FIR filters, IIR filters by Impulse invariance, bilinear transformation, FIR/IIR cascaded lattice structures.

Unit 2 :Multirate Digital Signal Processing (07 Hrs)

Multi rate DSP, decimators and interpolators, sampling rate conversion, multistagedecimator & interpolator, poly phase filters, QMF, digital filter banks, applications in subband coding.

Unit 3: Linear Prediction & Optimum Linear Filters(07 Hrs)

Linear prediction & optimum linear filters, stationary random process, forward-backwardlinear prediction filters, solution of normal equations, AR lattice and ARMA lattice-ladder filters, Wiener Filters for filtering and prediction.

SECTION-II

Unit 4: Adaptive Filters (07 Hrs)

Adaptive filters, applications, gradient adaptive lattice, minimum mean squarecriterion, LMS algorithm, recursive least square algorithm

Unit 5: Power Spectrum Estimation (07 Hrs)

Estimation of spectra from finite-duration observations of signals, nonparametricmethods for power spectrum estimation, parametric methods for power spectrum estimation, minimum-variance spectral estimation, Eigen analysis, algorithms for spectrum estimation.

Unit 6:Wavelet Transform & Application of DSP (07 Hrs)

Application of DSP & multi rate DSP, application to radar, introduction to Wavelets,application to image processing, design of phase shifters, DSP in speech processing & other applications

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- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum

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- **Reference Books**

1. J.G.Proakis and D.G.Manolakis, "Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007
2. N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999
3. Sanjit K Mitra ,"Digital Signal Processing-A Computer Bases Approach",3rd Edition McGraw Hill,2009
4. M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons Inc., 2002
5. S.Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001
6. D.G.Manolakis, V.K. Ingle and S.M.Kogon, "Statistical and Adaptive Signal Processing", McGraw Hill, 2000

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

VOICE AND DATA NETWORKS

Teaching Scheme
Lectures –3Hours/week, 3 Credits
Tutorial –1 Hour/week, 1 Credit

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks
ICA – 25Marks

SECTION I

Unit 1-Network design issues- **(6 Hrs)**

Network design issues, network performance issues, network terminology, centralized and distributed approaches for network design, issues inn design of voice and data networks

Unit-2 Voice Networks **(6 Hrs)**

Layered and layer-less communication, cross layer communication, voice networks (wired and wireless) and switching, circuit switching and packet switching, statistical multiplexing.

Unit 3 Link layer protocols- **(8 Hrs)**

Data networks and its design, link layer design-link adaptation, link layer protocols, retransmission mechanisms-ARQ, hybrid ARQ, Go_back_N, selective repeat protocols and their analysis.

SECTION II

Unit 4- Communication across network- **(8 Hrs)**

Inter-networking, bridging, global internet, IP protocol and addressing, subnetting, classless inter domain routing (CDIR), IP address lookup, routing in internet, end to end protocols, TCP and UDP, congestion control, additive increase / multiplicative decrease. Slow start, fast retransmit / fast recovery.

Unit 5 Congestion control **(6 Hrs)**

Congestion avoidance, RED, TCP-throughput analysis, quality of service in packet networks, network calculus, packet scheduling algorithms

Unit 6 Network security- **(6 Hrs)**

Network security and management, principles of cryptography, authentication, integrity, key distribution and certification, access control and firewalls, attacks and measures

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. D. Bertsekas and R. Gallager, "Data Networks", 2nd Edition, Prentice Hall, 1992.
2. L. Peterson and B. S. Davie, "Computer Networks: A Systems Approach", 5thEdition, Morgan Kaufman, 2011.
3. Kumar, D. Manjunath and J. Kuri, "Communication Networking: An analytical approach"
   1st Edition, Morgan Kaufman, 2004.
4. Walrand,"Communications Network: A First Course", 2nd Edition, McGraw Hill, 2002.
5. William Stalling, "Network security, essentials", Pearson education Asia publication, 4th Edition, 2011

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

MACHINE LEARNING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA **–** 25Marks

SECTION-I

Unit 1: Introduction to Machine Learning **(06 Hrs.)**

Machine learning: what and why, supervised learning, unsupervised learning, some basic concepts in machine learning, definition of learning systems, goals and applications of machine learning, aspects of developing a learning system: training data, concept representation, function approximation

(Chapter 1 from Book 1, Chapter 1 from Book 2)

Unit 2: Linear and Logistic Regression **(08 Hrs)**

Linear regression: introduction, model specification, maximum likelihood estimation (least squares), robust linear regression, ridge regression, Bayesian linear regression, logistic regression: introduction, model specification, model fitting, Bayesian logistic regression, online learning and stochastic optimization, generative vs discriminative classifiers.

(Chapter 7 and 8 from Book 2)

Unit 3:Decision Tree Learningand Ensemble Methods **(08 Hrs)**

Representing concepts as decision trees, recursive induction of decision trees, picking the best splitting attribute: entropy and information gain, searching for simple trees and computational complexity, Occam's razor, overfitting, noisy data, and pruning, ensemble methods: bagging and boosting

(Chapter 3 from Book 1, Chapter 14 from Book 3)

SECTION-II

Unit 4: Clustering **(05 Hrs)**

Introduction, dirichlet process mixture models, affinity propagation, spectral clustering, hierarchical clustering, dlustering data points and features

(Chapter 25 from Book 2)

Unit 5: Sparse Kernel Machines **(05 Hrs)**

Introduction to Support Vector Machines (SVM), maximum margin classifiers, relevance vector machines, applications of Support Vector Machines

(Chapter 7 from Book 3)

Unit 6: Neural Networks and Deep Learning **(08 Hrs)**

Feed-forward network functions, network training, error backpropagation, regularization in neural networks, deep learning: introduction, deep neural networks, applications of deep networks

(Chapter 5 from Book 3, Chapter 28 from Book 2)

Unit 7: Key Ideas in Machine Learning **(04 Hrs)**

Introduction, key perspectives on machine learning, key results, where machine learning is headed next

(Chapter 14 of upcoming 2nd Edition of Book 1)

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 laboratory experiment based upon above curriculum

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- **Reference Books**

1. *Book 1*: Machine Learning by Tom Mitchell, McGraw Hill (1st Edition)
2. Draft content of chapter 14 of upcoming 2nd Edition of Book 1 http://www.cs.cmu.edu/~tom/mlbook/keyIdeas.pdf
3. *Book 2*: Machine Learning: a Probabilistic Perspective by Kevin Patrick Murphy
4. *Book 3*: Pattern Recognition and Machine Learning (Information Science and Statistics) by Christopher M. Bishop

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

ELECTIVE I: WIRELESS SENSOR NETWORKS

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA **–** 25Marks

SECTION-I

Unit 1: Introduction to Wireless Sensor Networks (WSN): **(06 Hrs.)**
Motivation, overview, network architecture, protocol stack, design objectives, challenges & constraints, technologies, hardware & software platforms, standards, applications

Unit 2: Medium Access Control (MAC): **(06 Hrs.)**
Overview of MAC, MAC for WSN- network characteristics, objectives, energy efficiency, contention MAC, contention free MAC, hybrid MAC

Unit 3: Routing & Clustering: **(08Hrs)**
Overview, challenges, metrics, data centric routing, proactive routing, on demand routing, hierarchical routing, location based routing, QoS based routing, introduction to clustering

SECTION-II

Unit 4: Node Architecture: **(04 Hrs.)**
Architecture, sensing, processing, communication interface, prototypes, software subsystems

Unit 5: Power Management: **(06 Hrs.)**
Need, classification, passive power conservation mechanism, active power conservation mechanism, power control at different protocol layer

Unit 6: Time Synchronization: **(04 Hrs.)**
Clocks and synchronization problems, basics of time synchronization, time synchronization protocols

Unit 7: Localization: **(04 Hrs.)**
Ranging techniques, range based localization, range free localization, event driven localization

Unit 8: Standards **(04 Hrs)**
IEEE 802.15- Overview, MAC layer, Zigbee- network layer, application layer

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. Wireless Sensor Networks – A Networking Perspective, Jun Zheng, Abbas Jamalipour, Wiley- IEEE
2. Fundamentals of Wireless Sensor Networks- Theory and Practice, WaltenegusDargie, ChrstianPoellabauer, Wiley
3. Networking Wireless Sensors, BhaskarKrishnamachari, Cambridge University Press
4. Wireless Sensor Networks- Technology, Protocols and Applications, KazemSohraby, Daniel Minoli, TaiebZnati, Wiley India
5. Wireless Sensor Network Designs, Anna Hac, John Wiley and Sons

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

ELECTIVE I: ANALOG AND DIGITAL CMOS VLSI DESIGN

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA **–** 25Marks

SECTION I

Digital CMOS Design

Unit 1: Review **(7 Hrs)**

Basic MOS structure and its static behavior, quality metrics of a digital design: cost, functionality, robustness, power, and delay, stick diagram and layout, wire delay models inverter: static CMOS inverter, switching threshold and noise margin concepts and theirevaluation, dynamic behavior, power consumption.

Unit 2: Physical Design Flow: **(7 Hrs)**

Floor planning, placement, routing, CTS, power analysis and IRdrop estimation-static and dynamic, ESD protection-human body model, machine model.

*Combinational logic***:** Static CMOS design, logic effort, ratioed logic, pass transistor logic, dynamic logic, speed and power dissipation in dynamic logic, cascading dynamic gates,CMOS transmissiongate logic.

Unit 3: Sequential Logic **(8 Hrs)**

Static latches and registers, Bi-stability principle, MUX based latches,static SR flip-flops, master-slave edge-triggered register, dynamic latches and registers,concept of pipelining, pulse registers, non-bistable sequential circuit

Advanced technologies: giga-scale dilemma, short channel effects, high–k, metal gate technology, FinFET, TFET etc.

SECTION II

Analog CMOS Design:

Unit 4:Single Stage Amplifier **(8 Hrs)**

CS stage with resistance load, divide connected load, currentsource load, triode load, CS stage with source degeneration, source follower, commongatestage, cascade stage, choice of device models.

Differential Amplifiers: basicdifference pair, common mode response, differential pair with MOS loads, Gilbert cell.

Unit 5: Passive and Active Current Mirrors: **(6 Hrs)**
Basic current mirrors, Cascade mirrors, Active currentmirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascadestage and difference pair, Noise

Unit 6: Operational Amplifiers: **(7 Hrs)**
One stage OPAMP, two stage OPAMP, gain boosting, commonmode feedback, slew rate, PSRR, compensation of 2 stage OPAMP, other compensationtechniques.

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",
   a. TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

ELECTIVE I: IMAGE AND VIDEO PROCESSING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA **–** 25Marks

SECTION I

Unit1: Image and Video Fundamentals :(04 Hrs.)

Image and video formats, Sampling in 2-dimension (2-D) and 3-dimension (3-D), image processing operations, digital video basics

Unit 2: Image Transforms: (06 Hrs.)

2D orthogonal & unitary transforms, discrete Fourier transform (DFT), discrete cosine transform (DCT), Hadamard transform, Haar transform, wavelet transform, Karhunen-Loeve transform (KLT), Singular value decomposition (SVD) transform.

Unit 3: Image and Video Enhancement (06 Hrs.)

Histogram, Point processing, spatial operations, transform operations, multi-spectral image enhancement, fundamentals of 2-D motion estimation and motion compensation, algorithms for 2-D motion estimation, motion-compensated filtering, frame rate conversion, deinterlacing

Unit 4: Image and Video Restoration (06 Hrs.)

Image observation models, inverse & Wiener filtering, generalized inverse, SVD and iterative methods, maximum entropy restoration, Bayesian methods, blind de-convolution, modeling in case of video restoration, intraframe shift invariant restoration, multiframe restoration

Section– II

Unit 5:Image and Video Segmentation (06 Hrs.)

Discontinuity based segmentation- line detection, edge detection, thresholding, region basedsegmentation, scene change detection, spatiotemporal change detection, motion segmentation, simultaneous motion estimation and segmentation, semantic video object segmentation

Unit 6:Image and Video Compression (06 Hrs.)

Lossless image compression including entropy coding, lossy image compression, videocompression techniques, international standards for image and video compression (JPEG, JPEG 2000, MPEG-2/4, H.264, HEVC), video quality assessment

Unit 7:Image analysis & computer vision (06 Hrs.)

Spatial feature extraction, transform features, edge detection, boundary extraction, boundary representation, region representation, moment representation, structure, shape features, texture, scene matching & detection, image segmentation, classification techniques.

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. Fundamentals of Digital Image Processing, K. Jain, Pearson education(Asia) Pte. Ltd. / Prentice Hall of India, 2004
2. Handbook of Image & Video Processing, Al Bovik, Elsevier Academic Press, 2nd Edition
3. Multidimensional Signal, Image and Video Processing and Coding, John W. Woods, Academic Press, Elsevier, 2006.
4. Fundamentals of Multimedia, Z. Li, M.S. Drew,Pearson education (Asia) Pte. Ltd., 2004
5. Digital Image Processing,R. C. Gonzalez, R. E. Woods, Pearson education (Asia) Pte. Ltd. /Prentice Hall of India, 2004, 2nd Edition
6. Digital Video Processing, M. Tekalp,Prentice Hall, USA, 1995

Solapur University, Solapur

M.Tech. (Electronics) Semester-I

ELECTIVE I: NEURAL NETWORKS AND FUZZY CONTROL SYSTEMS

Teaching Scheme	Examination Scheme
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION I

Unit1: Artificial neural system-preliminaries:(04 Hrs)

Neural computations, models of artificial neural networks (ANN), neural processing, learning and adaptation, learning rules, applications of ANN

Unit2: Feed-forward ANN and supervised learning: (07 Hrs.)

Single layer perception classifiers- continuous, discrete, multi category, multilayer feed-forward, error back propagation, learning factors, variants of back propagation, ANN as a statistical recognizer

Unit 3:Recurrent neuro-dynamical systems:(05 Hrs.)

Discrete time Hopfield ANN, gradient type Hopfield ANN, content addressable memory, simulated annealing, Boltzman machine, bidirectional associative memory

Unit 4:Identification, control and estimation using ANN:(04 Hrs.)

Linear system identification, autoregressive model, ARMA model, nonlinear system modeling, identification of control of nonlinear dynamical systems, independent component analysis, spectrum estimation, case studies

SECTION- II

Unit 5:Fuzzy control-preliminaries:(07 Hrs.)

Fuzzy sets, fuzzy relations, approximate reasoning, representing a set of rules, membership functions, fuzzy controller from industrial perspective, knowledge based system for process control, knowledge representation, applications of fuzzy logic

Unit 6:Fuzzy controller design:(07 Hrs.)

Structure of fuzzy controller, rule base, data base, inference engine, fuzzification and defuzzification, nonlinear fuzzy control, PID like fuzzy controller

Unit 7:Fuzzy nonlinear simulation: (06 Hrs.)

Relational equations, partitioning, non linear simulation using fuzzy rule based systems, fuzzy associative memories

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. Neural Networks- Classroom Approach, Satish Kumar, Tata McGraw-Hill Publishing Company Ltd.
2. Introduction to Artificial Neural Systems, Jacek M Zurada, Jaico Publishing House
3. Principles of Neurocomputing for Science and Engineering, Fredric M Ham, Ivica Kostanic, Tata McGraw-Hill Edition
4. Neural Networks and Learning Machines, Simon Haykin, Prentice Hall of India Pvt. Ltd.
5. An Introduction to Fuzzy Control, DimiterDriankov, Hans Hellendoorn, Michael Reinfrank, Narosa Publishing House
6. Fuzzy Logic with Engineering Applications, Timothy J. Ross, McGraw Hill, Inc

Solapur University, Solapur

M.Tech. (Electronics) Semester-II

RESEARCH METHODOLOGY& IPR

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Tutorial –1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Research fundamentals: **(6 Hrs.)**
Definition, objectives, motivation, types of research and approaches, research- descriptive, conceptual, theoretical, applied and experimental

Unit 2: The initial research process: **(6 Hrs.)**
Literature review, research design, assortment of the problem, identification of problem, defining a problem, objective, sub objective and scope, assumptions, validation criteria, research proposal(synopsis)

Unit 3: Report writing and presentation of results: **(5 Hrs.)**
Need, report structure, formulation, sections, protocols, graphs, tables, IEEE format, evaluation of report, writing abstract, writing technical paper

Unit 4: Information communication technology: **(3 Hrs.)**
Introduction, e-research, indices, virtual lab, digital lab, ethical issues in research

SECTION-II

Unit 5: Mathematical modeling and simulation: **(7 Hrs.)**
Mathematical modeling – need, techniques and classification, system models –types, static, dynamic, system simulation – why to simulate, technique of simulation, Monte Carlo simulation, types, continuous modeling, discrete model, role of probability and statistics in simulation, statistical distributions,

Unit 6: Nature of Intellectual Property: **(7 Hrs.)**
Patents, designs, trade and copyright, process of patenting and development: technological research, innovation, patenting, development, international scenario: international cooperation on intellectual property, procedure for grants of patents, patenting under PCT.

Unit 7: Patent Rights: **(6 Hrs.)**

Scope of patent rights, licensing and transfer of technology, patent information and databases, geographical indications

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- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum seven assignments based upon above syllabus

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- **Reference Books**

1. Fundamental of Research Methodology and Statistics, Yogesh Kumar Sing, New Age International Publishers
2. Research Methodology: Methods and Techniques, C.R. Kothari, New Age International Publishers, 2nd revised Edition
3. Research Methodology, Concepts and Cases, Deepak Chawla, NeenaSondhi, Vikas
4. Intellectual Propertyin New Technological Age, Robert P. Merges, Peter S. Menell, Mark A. Lemley, 2016.
5. Intellectual Property Rights by Neeraj Pandey And Khushdeep Dharn
6. Intellectual Property Rights Under WTO,T. Ramappa, S. Chand, 2008
7. Intellectual Property Rights Journal by CSIR-National institute of science Communication and Information Resources. (*January 2017 and March-May-2018*)

Solapur University, Solapur

M. Tech. (Electronics) Semester-II

COMMUNICATION BUSES AND INTERFACES

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical-2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Bus Systems **(5 Hrs)**
Serial Buses, physical interface, data and control signals, features.

Unit 2: Serial interfaces- **(8 Hrs)**
RS232, RS485, I^2C, SPI with their limitations and applications.

Unit 3: CAN in automation- **(7 Hrs)**
CAN - architecture, data transmission, layers, frame formats, applications

SECTION-II

Unit 4: Peripheral component interconnect- **(8 Hrs)**
PCI, PCIexpress - revisions, configuration space, hardware protocols and applications

Unit 5:Universal serial bus- **(6 Hrs)**
Transfer types, enumeration, descriptor types and contents, device driver

Unit 6:Data transfer- **(6 Hrs)**
Data streaming serial communication protocol- serial front panel data port (SFPDP) using fiber optic and copper cable

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- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiments based upon above curriculum

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- **Reference Books**

  1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition
  2. Jan Axelson, “USB Complete”, Penram Publications
  3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
  4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
  5. Serial Front Panel Draft Standard VITA 17.1 – 200x
  6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

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M.Tech. (Electronics) Semester-II

ADVANCED INTERNET OF THINGS (IoT)

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical –2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION- I

Unit 1: Introduction to IoT **(7 Hrs.)**

Smart cities and IoT revolution, Fractal cities, From IT to IoT, M2M and peer networking concepts, Ipv4 and IPV6

Unit 2:Communication Protocols **(7 Hrs.)**

Software defined networks SDN, from cloud to fog and MIST networking for IoT communications, principles of edge/P2P networking, protocols to support IoT communications, modular design and abstraction, security and privacy in fog.

Unit 3: Wireless Sensor Networks **(6 Hrs.)**

Introduction, IOT networks (PAN, LAN and WAN), edge resource pooling and caching, client side control and configuration

SECTION II

Unit 4: IoT Platforms. **(7 Hrs.)**

Smart objects as building blocks for IoT, open source hardware and embedded systems platforms for IoT, edge/gateway, IO drivers, C Programming, multithreading concepts

Unit 5:IoT Operating Systems **(7 Hrs.)**

Operating systems requirement of IoT environment, study of mbed, RIoT, and Contiki operating systems, introductory concepts of big data for IoT applications

Unit 6: Applications of IoT **(6 Hrs.)**

Connected cars IoT transportation, smart grid and healthcare sectors using IoT, security and legal considerations

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- **Internal Continuous Assessment (ICA)**
  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum.

- **Reference Books**

1. A Bahaga, V. Madisetti, “Internet of Things- Hands on approach”, VPT publisher, 2014.
2. The Internet of Things: Enabling Technologies, Platforms, and Use Cases", by Pethuru Raj and Anupama C. Raman (CRC Press)
3. Industry 4.0: The Industrial Internet of Things”, by Alasdair Gilchrist (Apress)
4. A. McEwen, H. Cassimally, “Designing the Internet of Things”, Wiley, 2013.
5. CunoPfister, “Getting started with Internet of Things”, Maker Media, 1st edition, 2011.
6. Samuel Greenguard, “Internet of things”, MIT Press, 2015.

Solapur University, Solapur

M.Tech. (Electronics) Semester-II

PLC, SCADA AND DISTRIBUTED CONTROL SYSTEMS

Teaching Scheme	Examination Scheme
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical –2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Automation fundamentals **(7 Hrs)**

Automation and its importance, automation applications, expectations of automation, process and factory automation. Types of plant and control- categories in industry, open loop and closed loop control functions, continuous, discrete and mixed processes, automation hierarchy – large control systems, data quantity, quality and hierarchical control. Control system architecture – evolution and current trends, comparison of different architectures

Unit 2:Programmable Logic Controller Hardware **(7 Hrs)**

Evolution of PLC, definition, functions of PLC, advantages and architecture, working of PLC, scan time, types & specifications, digital input, digital output, analog input, analog output examples and ratings, I/O modules, local and remote I/O expansion, communication modules & special purpose modules, memory and addressing – memory organization (system memory & application memory), I/O addressing, hardware to software interface.

Unit 3: PLC Programming **(7 Hrs)**

Software development of relay logic Ladder diagram, introduction to PLC programming, programming devices, IEC standard PLC programming languages, ladder diagram programming: basic instructions, PLC timers and counters: types and examples, data transfer & program control instructions, advanced PLC instructions, PID control using PLC. Case study: PLC selection and configuration for any one process applications.

SECTION-II

Unit 4:Distributed control System (DCS) **(7 Hrs)**

Introduction to DCS, evolution of DCS, DCS flow sheet symbols, architecture of DCS, controller, input and output modules, communication module, data highway, local I/O bus, workstations, specifications of DCS, DCS system integration with PLCs: HMI, man machine interface sequencing, supervisory control and integration with PLC, personal computers and direct I/O, serial linkages, network linkages, introduction to DCS programming, function block diagram method for DCS programming.

Unit 5:Supervisory Control and Data Acquisition Systems (SCADA) (7 Hrs)

SCADA: Introduction, brief history, elements of SCADA, features of SCADA, MTU- functions of MTU, RTU- functions of RTU, protocol details of SCADA- types and methods used, components, protocol structures and mediums used for communications, SCADA development for any one typical application, programming for GUI development using SCADA software.

Unit 6: Applications of PLC and SCADA (7 Hrs)

Systems block diagram, operation, ladder diagram and explanation for following applications: steam boiler control system using PLC, conveyer belt automation system, automation of bottle filling plant, material flow measurement systems and traffic light controller using PLC.

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiments based upon above curriculum

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- **Reference Books**

1. John. W. Webb & Ronald A. Reis, "Programmable Logic Controllers- Principles and Applications", PHI , 5th Edition, 2002
2. Frank D. Petruzella, "Programmable Logic Controllers", Mc Graw Hill Education, 4th Edition, 2016
3. Gary Dunning, "Introduction to Programmable Logic Controllers", Thomson Learning, Pck Edition 2001
4. Stuart Boyer, " SCADA : Supervisory Control And Data Acquisition", International Society of Automation publication, 4th Edition, 2009
5. Samuel M. Herb, "Understanding Distributed Processor Systems For Control", International Society of Automation Publication, 1st Edition 1999
6. Krishna Kant, "Computer Based Process control", PHI 2nd Edition 2010

Solapur University, Solapur

M.Tech. (Electronics) Semester-II

ELECTIVE II- MOBILE TECHNOLOGY

Teaching Scheme
Lectures –3 Hours/week, 3 Credits
Tutorial –1 Hours/week, 1 Credit

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks
ICA – 25Marks

SECTION-I

Unit 1: GSM System Overview: **(8 Hrs)**

GSM architecture, location tracking and call set up, security, data services, network signaling, MAP protocol and dialogue, mobility management, databases, failure restoration, overflow control, SMS protocol, international roaming, operations, administration and maintenance

Unit 2: General Packet Radio Services (GPRS): **(6 Hrs.)**

Functional groups, architecture, network nodes, interfaces, procedures, billing, mobility management, applications, EDGE

Unit 3: Wireless Application Protocol (WAP): **(6 Hrs.)**

Model, gateway, protocol, user agent profile and caching, wireless bearers, development toolkit, network and application environments, wireless markup language, telephony applications, MMS, other applications

SECTION II

Unit 4: Universal Mobile Telecommunication Services (UMTS): **(7 Hrs.)**

Migration path, air interfaces, URRAN architecture, speech call, packet data, handover, core network evaluation

Unit 5: CDMA 2000: **(7 Hrs.)**

Evaluation, network architecture and structure, radio network, 1xEVDO, 1xRTT

Unit 6: Security Issues in Mobile Technology: **(6 Hrs.)**

Information security, attacks, components of information security, security techniques and algorithms, security protocols, security models and frameworks

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum six assignments based upon above syllabus

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- **Reference Books**

1. Mobile Computing, Technology, applications and Service Creation, Asoke K. Talukder, Hasan Ahmed, Rupa R. Yavagal, Tata McGraw Hill Education Pvt. Ltd., 2nd Edition
2. 3G Wireless Networks, Clint Smith, Daniel Collins, Tata McGraw Hill Publishing Company Ltd., 2nd Edition
3. Wireless and Mobile Network Architecture, Yi-Bing Lin, ImrichChlamtac, Wiley India

Solapur University, Solapur

M.Tech. (Electronics Engineering) Semester-II

ELECTIVE-II: REAL TIME SYSTEMS

Teaching Scheme
Lectures: 3 hrs/week, 3 Credits
Tutorial: 1 hr /week, 1 Credit

Examination Scheme
ESE –70 Marks
ISE – 30 Marks
ICA- 25 Marks

SECTION I

Unit 1: Introduction **(7 Hrs)**

Introduction , issues in real time computing , structure & application of a real time system , task classes ,performance measures for real time systems, estimating program run times, task assignment and scheduling, classical uniprocessor scheduling algorithms, uniprocessor scheduling of iris tasks, task assignment ,modelling timing constraints

Unit 2:Programming Languages and Tools- I **(7 Hrs)**

Programming languages and tools, desired language characteristics, data typing, control & conditional structures, facilitating hierarchical decomposition, packages

Unit 3: Programming Languages and Tools -II **(7 Hrs)**

Run time (exception) error handling, overloading and generics, multitasking, low level programming, task scheduling, timing specifications, programming environments, run time support

SECTIONB II

Unit 4: Real Time Databases **(7 Hrs)**

Real time databases ,basic definition, real time vs general purpose databases, main memory databases, temporal data, transaction priorities, transaction aborts, concurrency control issues, disk scheduling algorithms, two phase approach to improve predictability , serialization consistency , databases for hard real time systems.

Unit 5:Real –Time Communication **(7 Hrs)**

Real time communication, communications media, network topologies protocols, fault tolerant routing, fault tolerance techniques, fault types, fault detection, fault error containment redundancy, data diversity, reversal checks, integrated failure handling.

Unit 6: Evaluation techniques **(7 Hrs)**

Reliability evaluation techniques, obtaining parameter values, reliability models for hardware redundancy, software error models, clock synchronization, clock, an on fault, tolerant synchronization algorithm, impact of faults, fault tolerant synchronization in hardware, fault tolerant synchronization in software.

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum six assignments based upon above syllabus

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- **Reference Books**

1. C.M. Krishna, Kang G. Shin, "Real – Time Systems", McGraw – Hill International Editions, 1997.
2. Rajib Mall, "Real-time systems: theory and practice", Pearson Education, 2007
3. S. T. Allworth and R. N. Zobel, " Introduction to real time software design", McMillan, 2nd Edition, 1987
4. R.J.A Buhur, D.L Bailey, "An Introduction to Real – Time Systems", Prentice – Hall International, 1999.
5. Philip.A.Laplante, "Real Time System Design and Analysis", Prentice Hall of India, 3rd

Solapur University, Solapur
M.Tech (Electronics) Semester-II
ELECTIVE II-VLSI IN SIGNAL PROCESSING

Teaching Scheme
Lectures: 3 hrs/week, 3 Credits
Tutorial: 1 hrs/week, 1 Credit

Examination Scheme
ESE –70 Marks
ISE – 30 Marks
ICA- 25 Marks

SECTION- I

Unit1: DFG Representation and Iteration Bound **(6 Hrs)**
Representations of DSP algorithms, data flow graph representations, critical path, loop bound, iteration bound, algorithms for computing iteration bound

Unit2: Pipelining and Parallel Processing **(6 Hrs.)**
Pipelining approach to reduce critical path, parallel processing to handle higher sample rates, power reduction computations, combined pipelining and parallel processing

Unit 3: Retiming **(8 Hrs.)**
Introduction to retiming, definitions and properties, solving system of inequalities, cut set retiming and pipelining, retiming for clock period minimization, retiming for register minimization

SECTION II

Unit 4:Unfolding **(6 Hrs.)**
Introduction to unfolding, algorithm for unfolding, properties of unfolding, applications of unfolding

Unit 5:Folding **(5 Hrs.)**
Introduction to folding, folding transformation, lifetime analysis for register minimization in folded architecture

Unit 6:Systolic Array Design **(5 Hrs.)**
Methodologies, family of systolic arrays (FIR filter) using linear mapping techniques, matrix – matrix multiplication

Unit 7:Bit Level Arithmetic Architectures **(4 Hrs.)**
Parallel multiplication with sign extension**,** parallel carry ripple array multipliers, parallel carry save array multipliers, parallel multipliers with modified booth recording

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- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum seven assignments based upon above syllabus

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Reference Books:

1. VLSI Digital Signal Processing Systems- Design and Implementation, Keshav K. Parhi, Wiely (India)
2. Architecture for Digital Signal Processing, Peter Pirsch, Wiley India
3. Digital Signal Processing in VLSI,Richard J. Higgins
4. VLSI Synthesis of DSP Kernels-Algorithmic and Architectural Transformations, Mahesh Mehendale, Sunil D. Sherlekar

Solapur University, Solapur
M.Tech. (Electronics) Semester-II
ELECTIVE II - ADVANCED CONTROL SYSTEMS

Teaching Scheme
Lectures –3 Hours/week, 3 Credits
Tutorial –1 Hours/week, 1 Credit

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks
ICA – 25Marks

SECTION- I

Unit1: State Space Analysis: **(7 Hrs.)**
State space representation, state transition matrix, response of LTI system, controllability & observability, state representation of discrete system, transfer function of z-domain

Unit2: Digital Control System: **(7 Hrs.)**
Sampling and quantization effects, zero order hold-block, frequency domain consideration, difference domain representation, analysis in Z domain, transfer function, & complete response

Unit 3: Stability analysis: **(7 Hrs.)**
Mapping between S-plane &Z-plane, justify stability criteria, steady state error and error constant, root locus, bode and analytical methods of design, Lyapunov stability

SECTION- II

Unit 4: Pole placement and observer design: **(7 Hrs.)**
State feedback gain, design via pole placement, state observers, observer design, servo systems, design of state & output regulations

Unit 5: MIMO control: **(7 Hrs.)**
Models for multivariable systems, basic MIMO control loop, closed loop stability, pairing of inputs and outputs, converting MIMO problems to SISO problems

Unit6: Robust control system: **(7 Hrs.)**
Introduction, system sensitivity, analysis of robustness, system with uncertain parameter, design of robust control system, design examples, robust internal model control system

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- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum six assignments based upon above syllabus

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- **Reference Books:**

1. Adaptive and Robust Control, Karl Astorm, Wittenmark, Pearson Education, 1995.
2. Robust Control, PatrosIonnav, Jing Sun, Prentice Hall of India Pvt. Ltd., 1996.
3. Discrete Time Control System, K.Ogata, Pearson Education, 2nd Edition,2001
4. Control System Design, G.C.Goodwin, Graebe , Salgado Prantice Hall of India Pvt. Ltd.2002.
5. Digital Control and State Variable Methods, M. Gopal, Tata Mc Graw Hill, 2 nd Edition, 2005
6. Digital Control Systems, V. I. George, C. P. Kurian, Cengage Learning, 1st Impression 2012